SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_XGa_{1-X}Se_2$-BASED SOLAR CELLS***

SUBCONTRACT NO: **NDJ-2-30630-18**

REPORT FOR: Phase III/Quarter 3

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This is the progress report for the 3rd quarter of Phase III of the above subcontract. The project deals with two thin film technologies: CdTe and CIGS. The focus areas include: (a) CdTe – stability, novel back/front contacts, and the development of manufacturing friendly processes; (b) CIGS – development of two-step non-co-evaporation technology.

Part I – CdTe

This report summarizes results from a stability study that focused on devices fabricated with varying amounts of Cu, in an effort to determine the role of this element on device stability and long term performance.

Initial Performance

The devices utilized in this study were fabricated with baseline procedures *excluding* the back contact fabrication step. The SnO_2 front contact, CdS, and CdTe were deposited by chemical vapor deposition, chemical bath deposition, and close spaced sublimation respectively; prior to the formation of the back contact the structures were also $CdCl_2$-heat treated. All these processes have been described in previous reports as part of the USF "baseline" device fabrication process. The only process variation was in the back contact: following the $CdCl_2$ heat treatment the structures were rinsed in methanol and etched in a Br_2 solution (0.1% vol. in methanol). Subsequently, a thin Cu film (thickness varied) was deposited by sputtering; following the Cu deposition a graphite electrode was applied and heat treated in inert ambient. No intentional dopant was included in the graphite (used as-received); it is possible that the overall fabrication process could be re-optimized around this particular contact process for better initial performance, something that was not attempted for this work.

Figure 1 shows the initial performance characteristics of the solar cells used in this study; these were fabricated with different amounts of Cu in the back contact (see Fig.1) and heat treated at 240°C. The V_{OC}'s are reproducible and appear to improve with decreasing Cu thickness; however the FF's exhibit significant dispersion for the two larger Cu thicknesses, the cause of which is not clear at this time. Light soaking of the cells was carried out in a vacuum oven under N_2 ambient (the experimental set up was described in a previous report); the cells were exposed to light (within ±15% of AM1.5) during a 4 hour interval (ON), and subsequently stored

in the dark for another 4 hours (OFF). Typically, four identical cells were stressed; two at open-circuit (OC) and two at short-circuit (SC) conditions; the cell arrangement is shown in Fig 2. Dark and light J-V were measured at regular intervals during the ON and OFF cycles (typically 8 measurements were taken during the ON cycle); light J-V measurements were taken at operating temperatures – which reached the 60-70°C range.

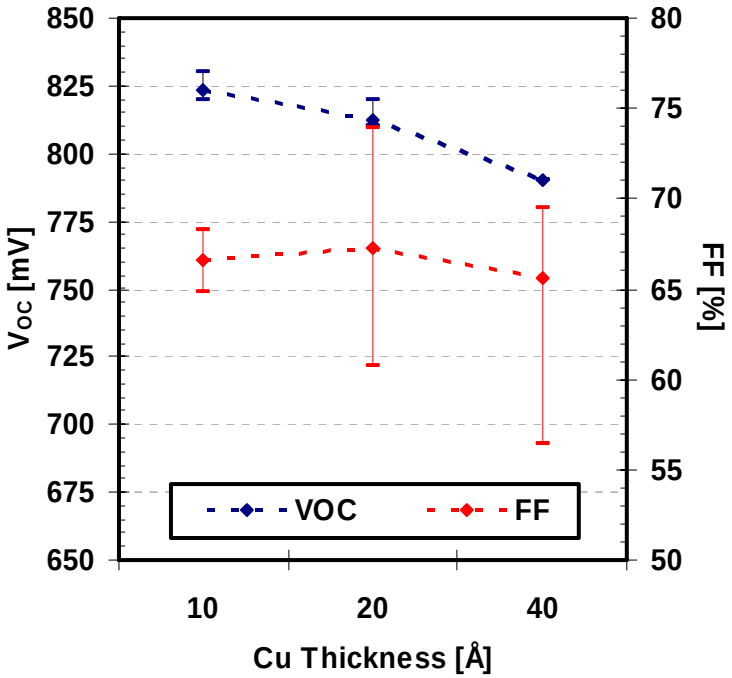


Figure 1. V_{OC} and FF of CdTe cells used for light soaking

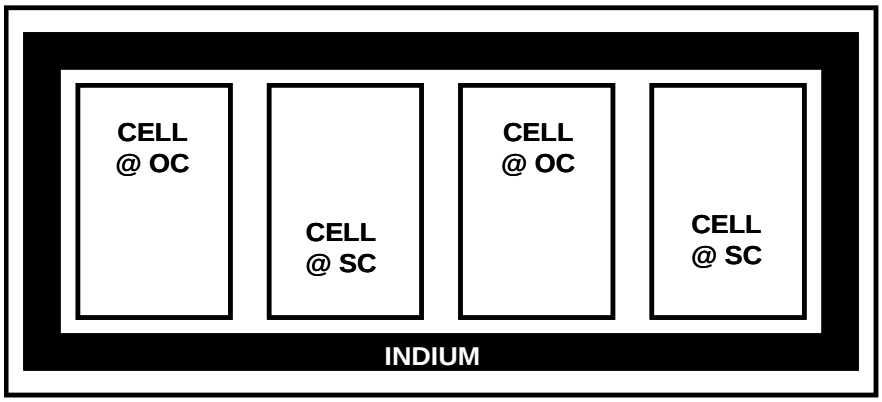


Figure 2. Substrate schematic showing the cell bias conditions

General Trends

Figure 3 shows the general trends for V_{OC} and FF for devices light-soaked for over 700 hours at OC and SC conditions (two devices at each condition); missing data indicates that the particular device most likely experienced a catastrophic failure; in some cases the soldered contact to the cell failed and had to be reconnected, which resulted in missing data over short periods of the light soaking process. It should also be noted that the apparent "spread" in the values of the V_{OC} and FF is to first order associated with the cell temperature rising during the ON cycle;

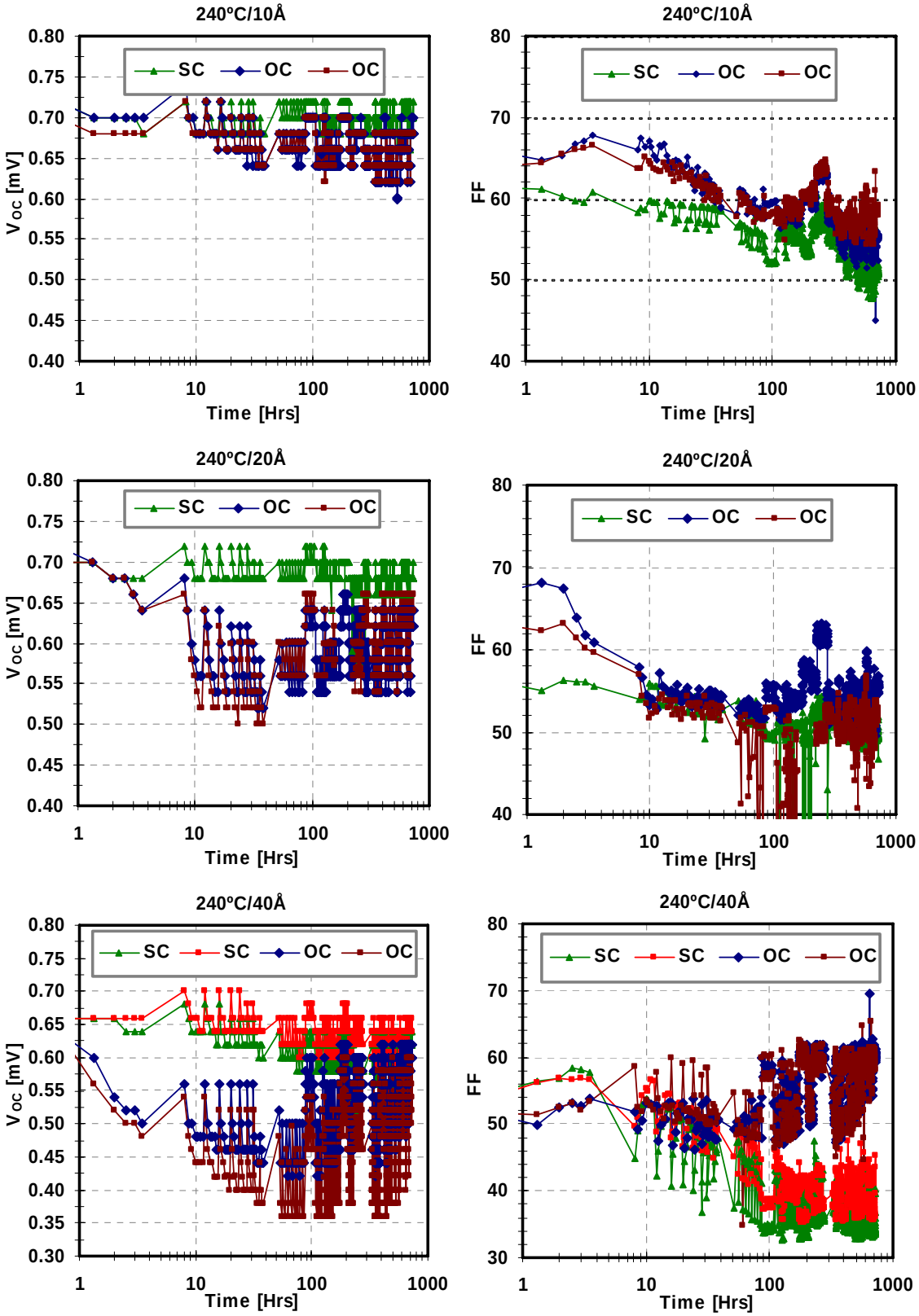


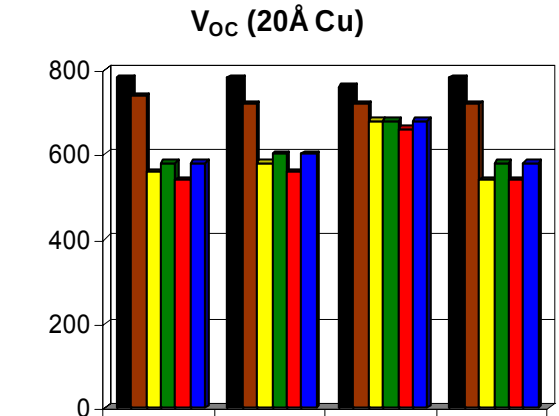
Figure 3. The V_{OC} and FF of CdTe cells during approximately 700 hours of light soaking; the back contact was formed using different amounts of Cu: top – 10Å; middle – 20 Å; bottom - 40 Å.

as indicted above up to 8 measurements were taken during the ON cycle, during which the sample temperature increased. Additional discussion on this variation will be provided below. The time axis in Fig. 3 is the total light soaking time (i.e. the time the cells were kept in the dark is not included).

Open Circuit Voltage - V_{OC}

As the data in Fig. 3 indicates cell performance decreased in all cases, however, there appear to be distinct differences among the three sets of devices as well as between the two bias conditions. The V_{OC} of the devices with the *smallest amount of Cu* (top/left) appears to have decreased slightly more for the devices held at OC but the difference is small, and since the number of devices tested is very small, it is considered to be insignificant. However, an examination of the two other sets of devices fabricated with increased Cu (left: middle and bottom), suggests that increasing the amount of Cu leads to two distinct changes: (a) *the **initial** (i.e. within the first 10-20 hours) decrease in V_{OC} increases with Cu*, and (b) the apparent "spread" in the values also seems to increase with Cu but only for the cells held at SC; more discussion on this "spread" will follow below. Therefore this set of data clearly suggests that higher Cu concentration is detrimental to V_{OC}, and the bias conditions influence the observed degradation; these observations are consistent with results obtained by other groups.

Some of the data of Fig. 3 are re-plotted in Fig. 4 to demonstrate two of the key general observations with respect to V_{OC}: (a) there is a large initial decrease, and (b) the overall decrease is larger for cells held at OC.



	OC	OC	SC	SC
initial	780	780	760	780
0.08	740	720	720	720
150	560	580	680	540
350	580	600	680	580
450	540	560	660	540
650	580	600	680	580

Figure 4. V_{OC} (in mV) for cells fabricated with 20Å of Cu; the left column shows the total hours

Fill Factor - FF

The general trend in the FF behavior varies significantly from that observed for V_{OC}. For the cell with the smallest amount of Cu (top/right), the initial and final (after 700 hours) values appear to be in the same range. However for cells held at OC there is an initial increase in the FF which is not uncommon for CdTe cells; this is consistent with findings of others who have observed an initial increase *in performance* during stability studies. As the Cu amount is increased (middle/right), the overall FF behavior appears to be very similar for both bias conditions (i.e. at OC and SC). Further increase in the amount of Cu leads to distinctly different trends for the FF of cells held at OC vs. SC; cells held at OC show an increase in the FF while those held at SC exhibit a decrease. As indicated earlier, from a performance point of view the devices fabricated with the largest amount of Cu exhibited the lowest performance, with the spread in the values of FF being significantly large.

The behavior of both the V_{OC} and FF suggests that the cells are undergoing changes that are not linear with time, and which can be quite complex; the higher Cu amounts clearly seem to lead to increased degradation as well as more complex behavior. From J-V data it is apparent that part of the FF losses can be attributed to increases in the series resistance, while losses in V_{OC} can be due to higher dark currents and/or collection losses. J-V data will be included in a future report.

"Transients"

In the previous section the presence of a "spread" in the V_{OC} values (to be referred to as a "transient" from this point onward) was attributed to the change in cell operating temperature. As already mentioned above, up to 8 measurements were taken during the ON cycles. During the ON cycle one would expect the cell temperature to rise, and initial calibrations of the sample stage suggested that the temperature of the cells could reach 60-70°C. It should be noted that only limited temperature data were collected during the light soaking process. Figure 5 shows smaller regions of the data shown previously in Fig. 3 (around 200 and 600 hours). The V_{OC} in all cases decreases during the duration of the ON cycle. When this "transient" behavior was first recorded it was attributed to the cell temperature rising and no further analysis was planned. However, as the light soaking process continued certain changes in the transient behavior seemed to suggest that this may not be simply a temperature effect; and the data suggests that a correlation exists between the transient and the amount of Cu and the bias condition. The magnitude of the V_{OC} *change* increases as one moves to higher Cu concentrations (it is highest for cells held at OC), and seems to decrease with time. Each plot in Fig. 5 (and Fig. 3) contains data from cells fabricated on the same substrate, and as indicated in Fig. 2 the bias conditions were alternated (i.e. the 1st and 3rd devices were held at OC and 2nd and 4th were held at SC); therefore the temperature of the four devices should be essentially identical. Nevertheless, the magnitude of this V_{OC} transient for the 40 Å devices (bottom) is clearly at least 2x higher for the cells light soaked at OC. To further demonstrate that this transient is not simply a temperature effect Fig. 6 shows the FF for the 40 Å. The FF behavior is again more complex. Around 200 hours the FF for the device held at OC decreases, while for the device held at SC it decreases and then recovers. At the 600 hour interval the device held at SC no longer shows any transient behavior, while the time constant of the transient of the device held at OC appears to be short.

In general the transient behavior can be attributed to trapping (and detrapping) of carriers through Cu-related (or possibly other impurity) complexes. Although the limited set of data collected in this case suggests a correlation with Cu, further targeted studies will be needed to possibly identify the complexes and their location across the device structure; it is also possible that these transients can be used to predict module long term stability.

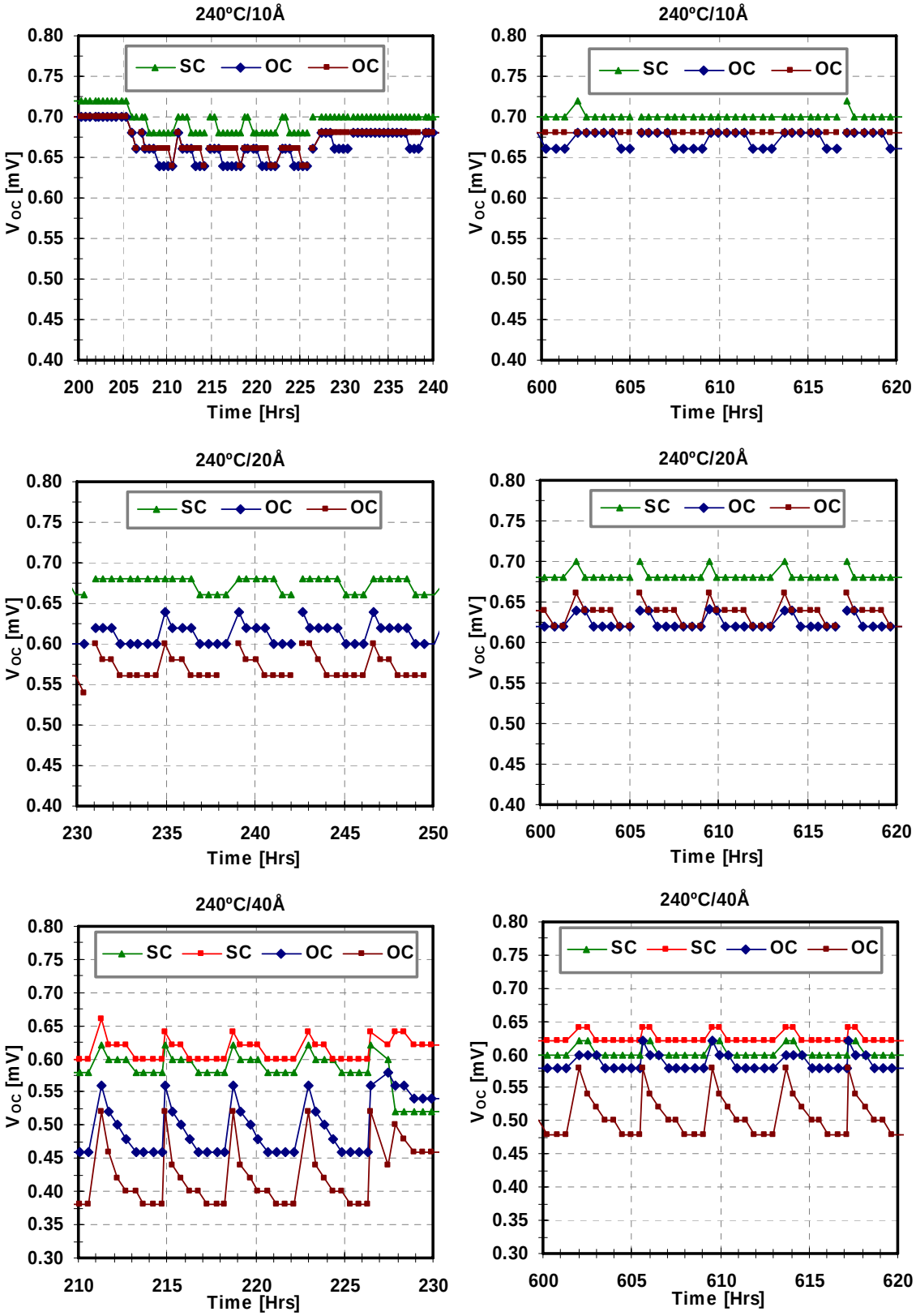


Figure 5. The data shown in this figure are expanded portions of the V_{OC} plots shown in Fig. 3, to show the variation of V_{OC} during the ON Cycle; data from 210-230 hours for the 20 Å cell were lost due to a break in the connection to the data acquisition system.

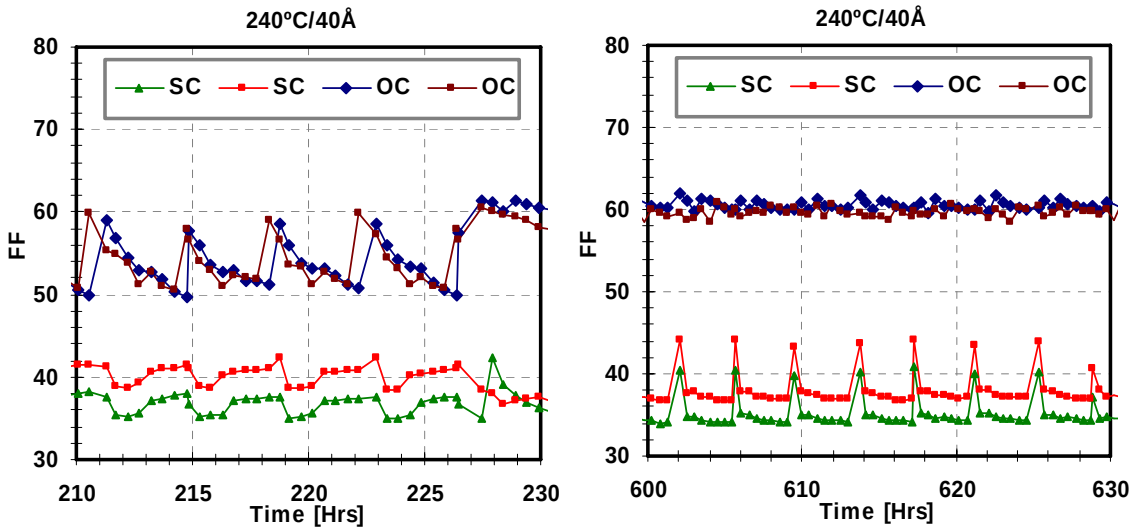


Figure 6. The FF for the 40 Å devices around the 200 and 600 hour

A complete set of J-V data for the above devices will be included in a future report.

It should also be noted that data from another set of devices, currently under light soaking, is also suggesting that Cu must be minimized for improved long term stability. The same results also suggest that to a great extent the observed degradation in CdTe devices may be improved and possibly eliminated if no Cu is used for the back contact formation. More on these results will be included in future reports when all results are available.

Part II - CIGS

Thickness Studies

Because of the recognized need to use less In in our devices we have initiated a study of the effects of reducing device thickness. Since our 2-step fabrication process depends upon judicious movement of deposited precursors to find their way to each other in the right proportions we expect that we will be confronted with not only the expected device level issues but with material formation issues as well. The formation of the CIGS absorber with our process involves tuning of process details to favor formation of the proper species over others that are equally apt to form. This has proven to be difficult and to date has not produced efficiencies on a par with the best co-evaporated devices. Recently we discussed the self-limiting mechanisms that were resulting in V_{OC} – J_{SC} tradeoffs that were pinning our device efficiencies[1]. An additional reason for reducing device thickness is that we expect additional insights into these mechanisms to evolve. Better understanding of these mechanisms will add to our ability to overcome them.

Experimental

Devices are prepared using our standard all-solid-state, 2-step process. The key processing detail for these studies is the manner in which the thickness is reduced. To reduce the thickness to half of the normal thickness we of course deposit half the amount of the metal constituents. However, this also affects the time/temperature profile. This as well as the Se flux level becomes a processing variable that must be optimized for each thickness used. These parameters will be addressed in future experiments.

1.5 Micron Thickness

Our standard device thickness is 2 microns. In our first experiment we reduced the device thickness to 75% of the standard thickness or to 1.5 microns. While there was a slight increase in V_{OC} relative to standard devices, the biggest effect was a 10% decrease in J_{SC}. In our last quarterly report we discussed the effects of annealing our devices at various stages, in particular after CdS and ZnO-i layer deposition. We concluded that the interface region was playing a dominant role in determining J_{SC} and that the ZnO-i layer had the greatest influence on J_{SC}. This was manifested as upward or downward movement of the QE spectrum. The QE spectrum for these devices relative to standard thickness is shown in Fig. 7. As can be seen, there is a downward shift in QE that is characteristic of interface effects. Thus the 10% drop in J_{SC} observed for 1.5 microns thickness is not due to the reduced thickness per se, so we are tentatively considering some relationship between the CIGS thickness and the properties of the ZnO-i interface region.

1.0 Micron Thickness

Reducing the thickness to 1 micron produces an additional effect as seen in Fig. 8 which contains spectra for four of the 1 micron devices and that of the standard thickness device. In addition to the downward shift in QE there is clearly a shift to higher band gap. The following is a tentative explanation. From previous results we know that most of the Ga resides at the rear of the device. In fact, it is difficult to form high band gap material in the space charge region. We expect then that because the bulk CIGS is now thinner it is easier for additional Ga to remain and bond in the space charge region, and this results in the increased band gap. Unfortunately this also causes additional reduction in J_{SC}. The reduction due to band gap shift is expected and all things being equal should be compensated by increased Voc. However, our experience has been that as we get the band gap to open, there are further reductions in J_{SC}, and that is the

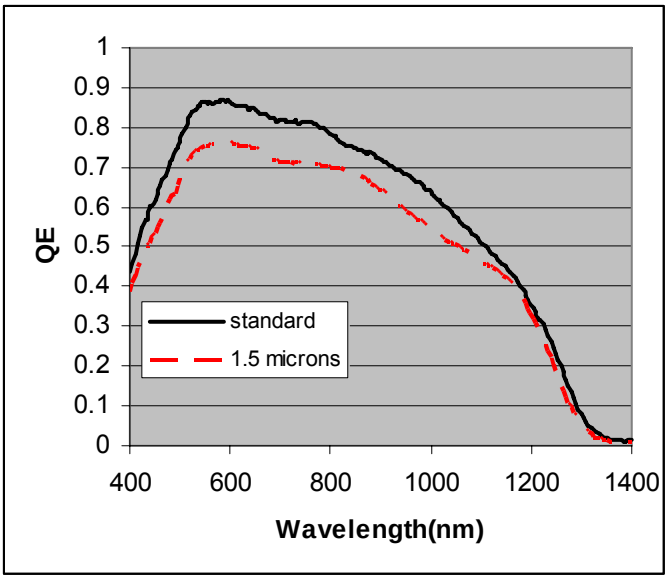


Figure 7. QE profiles for a standard thickness (2 microns) device and 1.5 microns device thickness

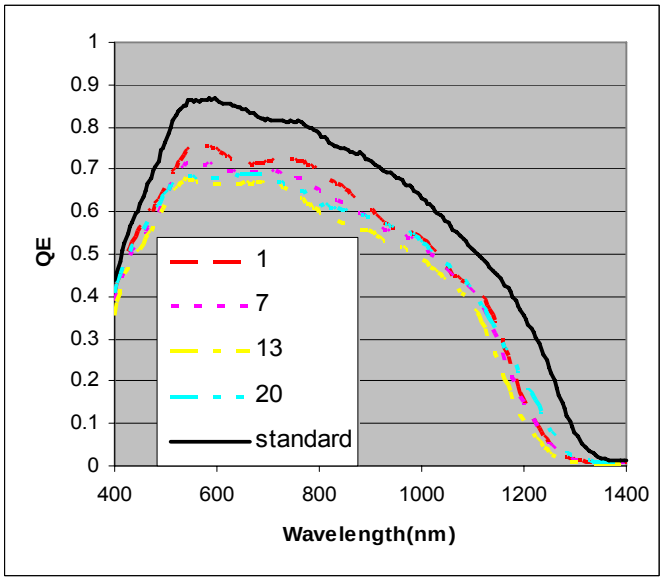


Figure 8. QE profiles for 1.0 micron device

case here. A closer examination of the QE spectra of Fig. 8 reveals that the device with the largest band gap shift, number 13, also has the lowest J_{SC}.

In Figs 9 and 10 we show the dependence of V_{OC} on both Cu/In and Ga/Se ratios. The data points are averages of 5 devices for each ratio. The exact ratios aren't provided, but devices at position 1 in Fig. 9 have a high Cu content, while at position 5 Cu is low and In is high(Cu/In range is typically 1.0 – 0.9). Similarly devices at position 1 in Fig. 10 have high Ga content, while those at 5 have lower Ga and higher Se. First of all the data in Fig. 10 show no clear trend. If Ga is an issue for J_{SC}, it is less of an issue for V_{OC}. However, there is clearly a trend for Cu/In composition. One might expect this to be driven by the bandgap, but that is not the case. In fact device 13 with the largest bandgap in Fig. 8 has only an average V_{OC} of 440 mV. While

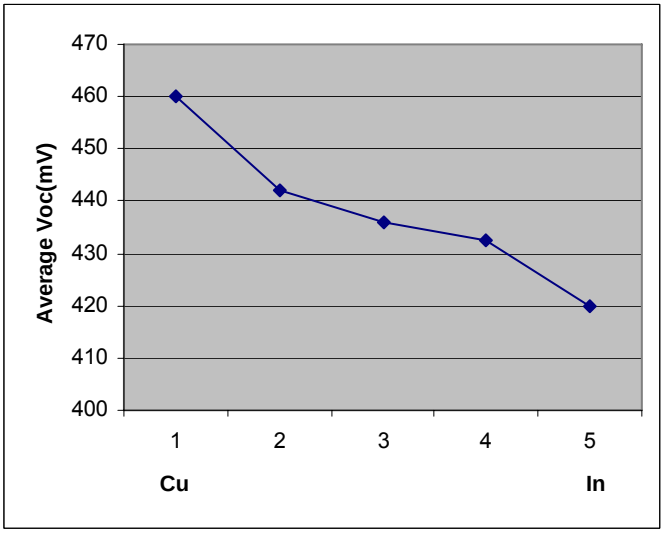


Figure 9. V_{OC} dependence vs. Cu/In for 1 micron thick devices

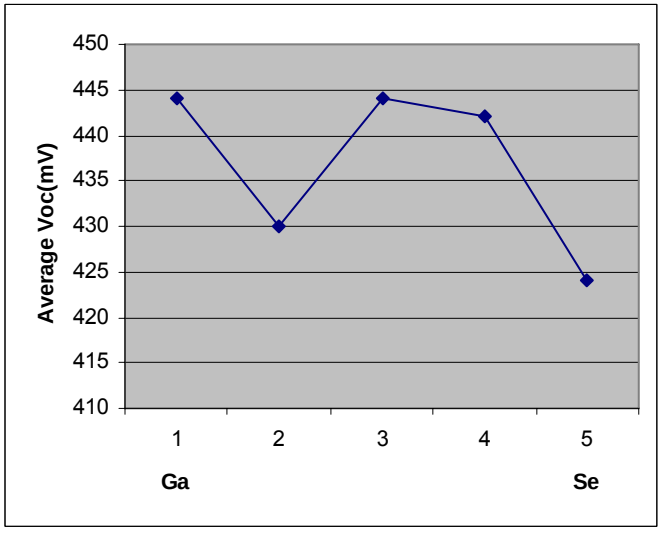


Figure 10. V_{OC} dependence vs. Ga/Se for 1 micron thick devices.

bandgap is playing a role, it would seem that it is being dominated by the influence of defects. That is, while the V_{OC} of a device with a larger band gap would benefit from the bandgap, if in increasing the bandgap the defect level were raised significantly, the adverse effect of the defects could override the bandgap effect. Thus the results of Fig. 9 suggest that 1 micron thick devices with higher Cu/In ratios have fewer defects. We have seen this effect before in standard thickness devices and are not surprised.

The following hypothesis emerges from these results. In thinner devices more Ga enters the space charge layer which opens the band gap. This nevertheless hurts V_{OC} because of the additional defects produced by the extra Ga. This also hurts J_{SC}. Devices with higher Cu/In have higher V_{OC} because they also have higher Cu/Group III ratios in the space charge region which holds down defect formation. While this gives us a procedure for maintaining V_{OC}'s as we go thinner, unfortunately the 10% loss in J_{SC} remains.

Since Ga entering the space charge layer seems to be the culprit here, we thought to provide additional In to prevent this from happening. In the next run we increased the In thickness from 1550 Å needed to proportionally achieve 1 micron to 1800 Å. As seen in Fig. 11 the band gap is still high indicating that the same amount of Ga is still bonding in the space charge region. This is surprising in that most of our observations indicate that Ga does not compete well with In and usually needs some help to enter the lattice. The J_{SC}'s are down a bit more here indicating that the extra In is contributing to defect formation. However, it is surprising that the devices can tolerate that much additional In. This also shows up in V_{OC}. The entire 5 x 5 array for V_{OC}'s is shown in Fig. 12. As can be seen, V_{OC} is at a respectable level of about 440 - 450 mV and there are no obvious compositional dependences. The results to this point suggest strong compensating mechanisms that allow for large fluctuations in composition but at the same time limit performance on the up side.

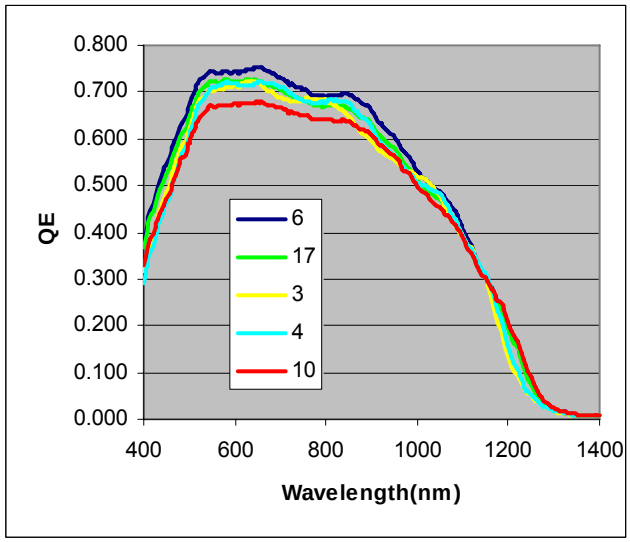


Figure 11. QE spectra for five 1 micron thick devices with extra In

Substrate Effects

In earlier studies we demonstrated that substrate effects, particularly Na, had to be factored into all experimentation[1]. Compensation mechanisms determine performance, and constituents from the substrate contribute to this process. To address this issue the Mo thickness was increased from 1 micron to 1.5 microns in an otherwise standard run of 1 micron CIGS. This is expected to lower the amount of Na entering the film, and we have observed changes in standard thickness devices using this technique[1]. For standard devices changes in J_{SC} and V_{OC} occur when more Na is admitted to the film by decreasing the Mo thickness. An increase from 1 micron to 1.5 microns produces no change, as the Na is properly regulated for thickness greater than 1 micron. Our thinking here was that because the CIGS is thinner the amount of Na entering the film for a 1 micron Mo layer might be too high. However, the results were negative. The device performance with the 1.5 micron Mo layer was identical to that for a 1 micron Mo layer. Although this is just one data point, we tentatively conclude that substrate effects are not

a dominant factor for thinner devices. This turns our attention back to the junction interface region. Several additional experiments are being planned to better understand the J_{SC} loss mechanism as we reduce device thickness.

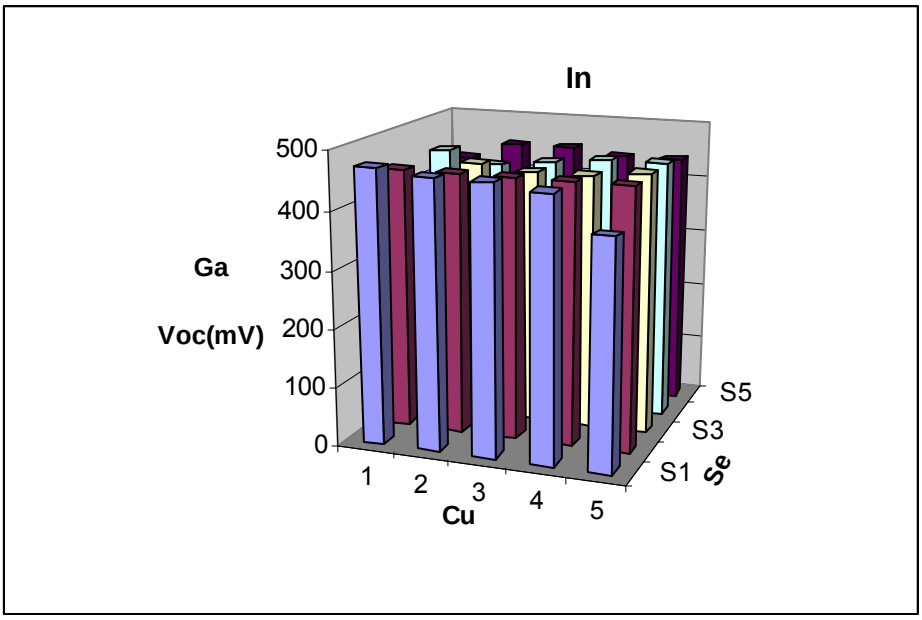


Figure 12. V_{OC} profile for 1 micron thick devices containing excess In

References

1. V. Mohanakrishnaswamy, H. Sankaranarayanan, S. Pethe, C. S. Ferekides and D. L. Morel, "The Effect of Mo Deposition Conditions on Defect Formation and Device Performance for CIGS Solar Cells", Proceedings of the 31st IEEE PVSC, Orlando, 2005.